REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-21 and 25-28 are pending in this application, Claim 29 having been canceled without prejudice or disclaimer; and Claims 1 and 25-27 having been presently amended. Support for amended Claims 1 and 25-27 can be found, for example, in the original claims, drawings and specification as originally filed.[1] No new matter has been added.

In the outstanding Office Action, Claims 1-9, 17, 19-21, and 25-29 were rejected under 35 U.S.C. § 103(a) as unpatentable over Aweya et al. (U.S. Patent No. 7,043,651; hereinafter "Aweya") in view of Zdepski (U.S. Patent No. 5,467,137); and Claims 10-16 and 18 were rejected under 35 U.S.C. § 103(a) as unpatentable over Aweya in view of Zdepski and Lahat (U.S. Patent No. 6,963,561).

In response to the rejection of Claims 1-9, 17, 19-21, and 25-29 under 35 U.S.C. § 103(a) as unpatentable over Aweya in view of Zdepski, Applicants respectfully submit that amended independent Claim 1 recites novel features clearly not taught or rendered obvious by the applied references.

Amended independent Claim 1 is directed to a method of synchronizing the phase of a local image synchronization signal generator including, *inter alia*:

> ...frequency synchronizing said local and reference clocks;
>
> said reference video data processor sending, via said network, to said local data processor ***one image timing packet providing reference image synchronization data indicating a difference in timing, measured with respect to said reference processor's clock, between a time at which said image timing packet is launched onto said network and a time of production of a reference image synchronization signal***; and

[1] See page 10, lines 7-20 of the specification.

said local video data processor controlling the ***phase of production of said local image synchronization signals in dependence on said reference image synchronization data and a time of arrival of said one image timing packet.***

Independent Claims 25-27 recite substantially similar features as independent Claim 1. Therefore, the arguments presented below with respect to Claim 1 are also applicable to independent Claims 25-27.

Zdepski describes a frequency synchronization scheme[2] in which, as outlined at column 2 lines 4-27, a transmitter embeds a count value in a signal on a predetermined schedule, and then additional packets include differential count values that represent delays incurred during the transmission process. At the receiver, the count value and differential value are added together. Also, at the receiver in Zdepski, a count value from a local counter is stored when the count value from the transmitter arrives. Finally, ***the differences of successive sampled count values*** from the transmitter and from the receiver are used to control the receiver clock[3] (i.e. to synchronize frequency, see column 5, lines 1-5 and the equation at column 5, line 1).

A person of ordinary skill in the art would therefore understand that Zdepski describes a system where multiple count values are used to synchronize frequency. However, Zdepski is completely silent on the issue of phase synchronization. In Applicants' Claim 1, ***one packet*** is used to achieve ***phase synchronization***. Thus, Zdepski fails to teach or suggest a "local video data processor controlling the ***phase of production of said local image synchronization signals in dependence on said reference image synchronization data and a time of arrival of said one image timing packet***," as recited in Claim 1.

Thus, Applicants' amended Claim 1 recites a method where, ***after*** frequency synchronizing of the local and reference clocks has occurred, ***one*** image timing packet is

[2] See Zdepski at column 1, lines 31-37.
[3] See Zdepski at column 2, lines 16-27.

transmitted that indicates the difference in time between a synchronization signal and the time at which that image timing packet is launched. At the local video data processor, the one image timing packet is used to control the timing (i.e. the phasing) of the local synchronization signal. Applicants respectfully submit that Zdepski fails to teach or suggest this process. In particular, Zdepski does not describe a phase synchronization method of ***any*** sort to follow its frequency synchronization method, and certainly does not describe the use of ***one*** timing packet to achieve such phase synchronization. Aweya describes the use of two timestamps in synchronization, and thus fails to cure any of the above-noted deficiencies of Zdepski.

Accordingly, Applicants respectfully submit that independent Claims 1 and 25-27 (and all claims depending thereon) patentably distinguish over Aweya and Zdepski, and Applicants respectfully request that the rejection of Claims 1-9, 17, and 19-29 under 35 U.S.C. § 103(a) be withdrawn.

In response to the rejection of Claims 10-16 and 18 under 35 U.S.C. § 103(a) as unpatentable over Aweya and Zdepski in view of Lahat, Applicants note that Claims 10-16 and 18 are dependent on independent Claim 1, and are thus believed to be patentable for at least the reasons discussed above. Further, Applicants respectfully submit that Lahat fails to cure any of the above-noted deficiencies of Aweya and Zdepski.

Accordingly, Applicants respectfully request that the rejection of Claims 10-16 and 18 under 35 U.S.C. § 103(a) as unpatentable over Aweya and Zdepski in view of Lahat be withdrawn.

Consequently, in view of the present amendment, and in light of the above discussion, the pending claims as presented herewith are believed to be in condition for formal allowance, and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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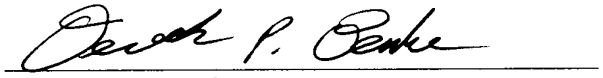

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